REMARKS

Claims 1-30 are pending in the application, of which claims 1, 14, 21, 29 and 30 are independent. Reconsideration and further examination are requested

Claim Rejections under 35 U.S.C. §101 (statutory subject matter)

The Examiner rejected claims 1, 14, 21, 29 and 30 under 35 U.S.C. § 101 as being directed to non-statutory subject matter.

While the Examiner rejected claims 1, 14, and 21 as being directed to non-statutory subject matter, to the best of Applicant's understanding it appears that the Examiner intended to reject claims 1, 14, and 21 as lacking utility. For example, in the rejections, the examiner states that no substantial practical application can be found. Applicant disagrees. Applicant's specification describes various uses and advantages of pushing a datum onto a stack and popping the datum off the stack. Accordingly, Applicant requests that the rejection of claims 1, 14, and 21 be withdrawn or that the examiner provide cogent reasons why this case is rejection under 35 U.S.C. 101.

The Examiner also rejected claims 29 and 30 under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Without conceding the appropriateness of the rejection, and solely to advance this application to issuance, Applicant has amended claims 29 and 30 as shown above. Accordingly, Applicant requests that the rejection of claims 29 and 30 be withdrawn.

Claim Rejections under 35 U.S.C. §101 (statutory type double patenting)

The Examiner rejected claim 2 under 35 U.S.C. §101 as claiming the same invention of that of claim 2 of U.S. Patent No. 6,631,462. Applicant has amended claim 1 from which claim 2 depends, so claim 2 is not coextensive in scope with claim 2 of U.S. Patent No. 6,631,462. Therefore, the Applicant requests withdraw of this rejection.

Claim Rejections under 35 U.S.C. §101 (nonstatutory obviousness-type double patenting)

The Examiner rejected claims 1, 14, 21, 29 and 30 under 35 U.S.C. §101 on the ground of non-statutory obviousness-type double patenting over claims 1, 14, 21 of U.S. Patent No. 6,631,462. Applicant has amended claims 1, 14, 21, 29 and 30. Therefore, Applicant requests withdraw of these rejections.

Claim Rejections under 35 U.S.C. §102

The Examiner rejected claim 1 under 35 U.S.C. §102(b) as being anticipated by LeBlanc (US 5,542,070). As amended, claim 1 recites "pushing a datum onto a stack by a first hardware-controlled processing thread in a hardware-based multi-threaded processor... and popping the datum off the stack by a second hardware-controlled processing thread in the hardware-based multi-threaded processor." Applicant's claim 1 is distinct over LeBlanc.

LeBlanc discloses a method of using object oriented programming to simulate a system on a computer.[1] In particular, LeBlanc discloses a method of compiling and interpreting code.[2] A code interpreter determines the interpretation and execution of different code segments, or "threads". However, the interpreter essentially operates as a conventional C language compiler that performs subroutine calls and returns. For example, LeBlank states:[3]

> In effect, xcolon has performed a transfer of control from the thread test to the thread "u." in a manner analogous to a subroutine call. At the completion of execution of the thread "u" control can be returned to the thread test using the value saved on the return stack.
>
> The inner interpreter then consecutively executes the code for each of the words specified in the thread for "u.". At the conclusion of the thread for u. the inner interpreter will execute the code associated with the reference to ";"--the C function xsemicolon This function pops the top of the return stack, placing the return address back into IP. This is analogous to a return from a subroutine call, and at the conclusion of this operation, xsemicolon returns control to the inner interpreter which will resume interpretation of the thread for test.
>
> At this point the end of the thread test has been reached and xsemicolon is called once again, returning control to whatever routine had originally invoked test.

[1] Col. 2, lines 13-15.
[2] Col. 8, lines 62-67.
[3] Col. 10, lines 13- 25, emphasis added.

As such, Leblanc's describes a software based system that uses object oriented programming to simulate a system. Leblanc does not teach or suggest a method that includes "pushing a datum onto a stack by a first hardware-controlled processing thread in a hardware-based multi-threaded processor... and popping the datum off the stack by a second hardware-controlled processing thread in the hardware-based multi-threaded processor" as recited by Applicant's claim 1.

Claims 2-13 depend from claim 1 and are patentable for at least the same reasons as claim 1.

Claim 14 includes a system that includes a first hardware-controlled processing thread in a hardware-based multi-threaded processor...including at least one command for pushing data onto the stack and a second hardware-controlled processing thread in a hardware-based multi-threaded processor... including at least one command for popping the data off the stack. For reasons similar to those described above, LeBlank, fails to disclose or suggest such a system. Applicant therefore requests reconsideration and withdrawal of the rejection of claim 14.

Claims 15-20 depend from claim 14 and are patentable for at least the same reasons as claim 14.

Claim 21 includes a stack module that includes control logic that responds to commands from at least two hardware-controlled processing threads in a hardware-based multi-threaded processor, the control logic storing datum on a stack structure in response to a push command and retrieving datum from the stack in response to a pop command. For reasons similar to those described above, LeBlank, fails to disclose or suggest such a stack module. Applicant therefore requests reconsideration and withdrawal of the rejection of claim 21.

Claims 22-29 depend from claim 21 and are patentable for at least the same reasons as claim 21.

Claim 29 includes a stack module configured to store data from a first hardware-controlled processing thread in a hardware-based multi-threaded processor by pushing the data onto a stack and to retrieve the data for a second hardware-controlled processing in the hardware-based multi-threaded processor thread by popping the data off the stack, the stack

module being responsive to a first processing thread command to store data on the stack and a second processing thread command to retrieve data from the stack. For reasons similar to those described above, LeBlank, fails to disclose or suggest such a stack module. Applicant therefore requests reconsideration and withdrawal of the rejection of claim 29.

Claim 30 includes an article that includes computer readable instructions for causing a processor to store data from a first hardware-controlled processing thread in a hardware-based multi-threaded processor by executing an instruction to push the data onto the stack and retrieve the data for a second hardware-controlled processing thread in the hardware-based multi-threaded processor by executing an instruction to pop the data from the stack for use by the second thread. For reasons similar to those described above, LeBlank, fails to disclose or suggest such an article. Applicant therefore requests reconsideration and withdrawal of the rejection of claim 30.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Respectfully submitted,

Date: 11/29/06

Tonya S. Drake
Reg. No. 57,861

Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

21474736.doc